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# A 10-bit, 200MS/s CMOS Pipeline ADC using new shared opamp architecture

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## Abstract

*A 10 bit opamp-sharing pipeline analog-to-digital converter (ADC) using a novel mirror telescopic operational amplifiers (opamp) with dual nmos differential inputs is presented. Reduction of power and area is achieved by completely merging the front-end sample-and-hold amplifier (SHA) into the first multiplying digital-to-analog converter (MDAC) using the proposed opamp. Transistors in the opamp are always biased in saturation to avoid increase of settling time due to opamp turn-on delays. The design targets 0.18um CMOS process for operation, at 200MS/s from a 1.8V supply. The simulation results show the SNDR and SFDR of 59.45dB and 68.69dB, respectively, and the power consumption of 35.04mW is achieved.*

## Keywords

*Analog to Digital converter (ADC), opamp sharing, high speed, low power, memory effect, pipeline*

## 1. INTRODUCTION

Many applications such as video detector and wireless communication systems, require high speed, low power, and high resolution analog-to-digital converters(ADCs) [1]. Since the required accuracy gradually decreases in the later stages of the pipeline architecture, the power consumption can be reduced by properly scaling the capacitor sizes and opamp transistors sizes (w/l) and bias current, without degrading the resolution of the ADC. Shared the opamp between two successive stages can further reduce power consumption and has been demonstrated to achieve good performance for low power operation [2]. The front-end sample and hold (S/H) is removed and 30% power is saved [3]. The block diagram of a 10b opamp-sharing pipeline ADC is shown in fig.1[5]. This architecture has two serious problems. First, because the opamp input summing node is never reset, unless a very long settling time is allowed: every input sample will be affected by the error voltage stored on the input capacitor due to the previous sample; thus it suffers from the memory effect, which can be considered as a kind of offset [4]. The ADC linearity can also be degraded by sharing the opamp. The memory effects can be alleviated by using dual differential input pairs opamps that operate in alternating phases [5]. Secondly, the parasitic capacitors of switches that are used to implement the opamp-sharing cause a potential

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cross talk path between two successive stages. In addition, the opamp-sharing switches also introduce input-dependent resistances and degrade the settling behavior [6], [7].

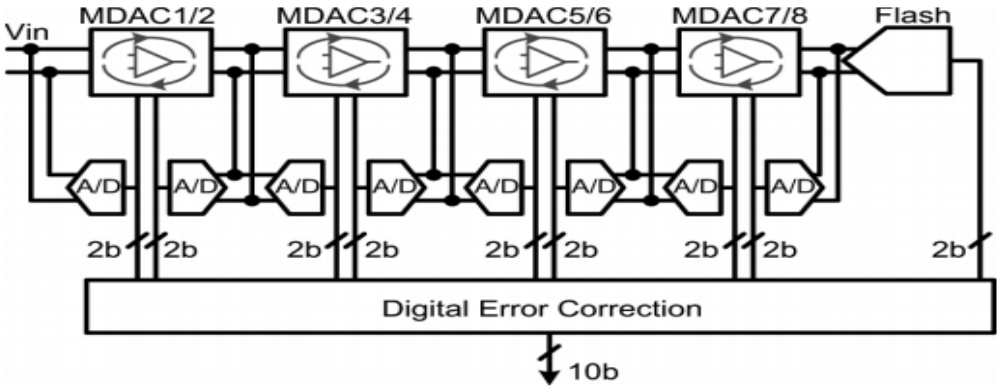


Figure 1. The block diagram of 10 b opamp-sharing pipeline ADC [5]

The dual differential inputs enable the opamp to be shared between successive stages without memory effect. Transistors in the opamp are always biased in saturation to avoid increase of settling time due to opamp turn-on delays [5]. The opamp-sharing technique in pipeline ADC is described in section 2 and the circuit implementation of the prototype 10b pipeline ADC is presented in section 3. Capacitor scaling method is described in section 4, and section 5 presents the simulation results. Concluding remarks are given in section 6.

## 2. OPAMP - SHARING PIPELINE ADC

In the high speed ADC, the power consumption is mainly determined by the opamps. To reduce the power consumption, we have to minimize the number of the opamps. The pipeline stage needs the opamp only during the amplification phase and not during the sampling phase. Therefore, during the sampling phase of one stage, the opamp can be shared with another stage. Fig.2 shows how an opamp is shared between two successive stages [3]. We use 1.5-bit per stage architecture. During the odd phase, when $\phi_1$ is high, the stage i samples the input voltage and stage i+1 amplifies the sampled output of the stage i. During the even phase, when $\phi_2$ is high, stage i+1 samples the output of stage i and stage i amplifies the sampled input. The opamp is used in stage i+1 in odd phase and in stage i during the even phase.

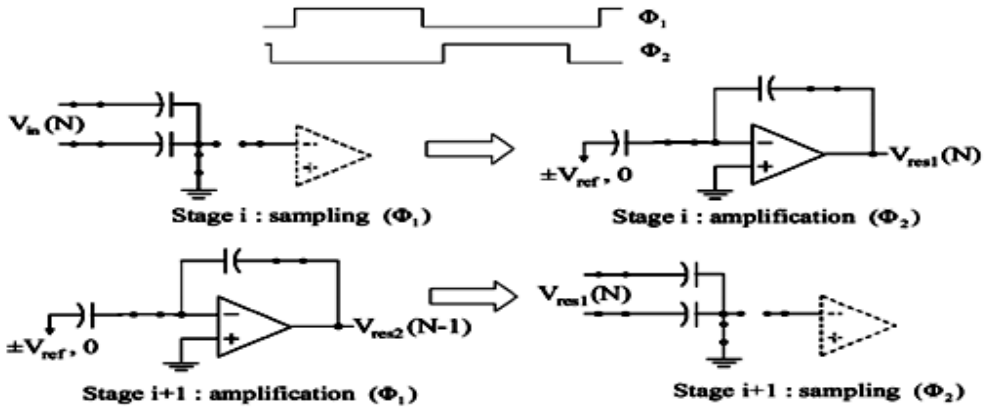


Figure 2. Opamp sharing between successive pipeline stages [3]

To eliminate the memory effect, caused by not resetting the opamp, dual differential inputs are used [7], [8]. When one input pair is being used for amplification, the other input pair is reset to common mode voltage avoiding the memory effect. As a consequence, since each pair is dedicated to an MDAC stage, additional switches are not required to implement opamp-sharing.

## 3. THE CIRCUIT IMPLEMENTATION

### 3.1. Proposed opamp

The schematic of the first and the second stages of the proposed opamp is shown in fig.3 and fig.4, respectively. The differential current generated from the input pair is copied to the output branch through a cascode current mirror. This topology achieves good gain, comparable to conventional telescopic opamp. Since input $g_m$ gets directly multiplied by k ( is shown in schematic and is mirror coefficient), it can be caused to achieve the same unity gain bandwidth with a better current efficiency comparable to telescopic opamp. the noise contribution of the cascode transistors is also very small and hence can be ignored. To achieve 10 bit accuracy, large amount of DC gain is required. To meet this requirement, two stage current mirror with a source follower to achieve high swing is used. Opamp comprises of nmos transistors M0-4 and switch S1. In clock phase $\phi_1$, the switch S1 is closed selecting M3-4 as the opamp input differential pair and the gates of M1-2 are biased to $V_{cm1}$. In the $\phi_2$, S1 is opened, selecting the M1-2 as the opamp input differential pair, and the gates of M3-4 are biased to $V_{cm2}$. For biasing the selected input differential pairs, the M0 is continuously biased and opamp is reused in both clock phases. To compensate for stability, we use the cascode compensation instead of mirror compensation [5]. V0-V5 used for the first and the second stages of the opamp are bias voltages to hold the transistors in saturation.

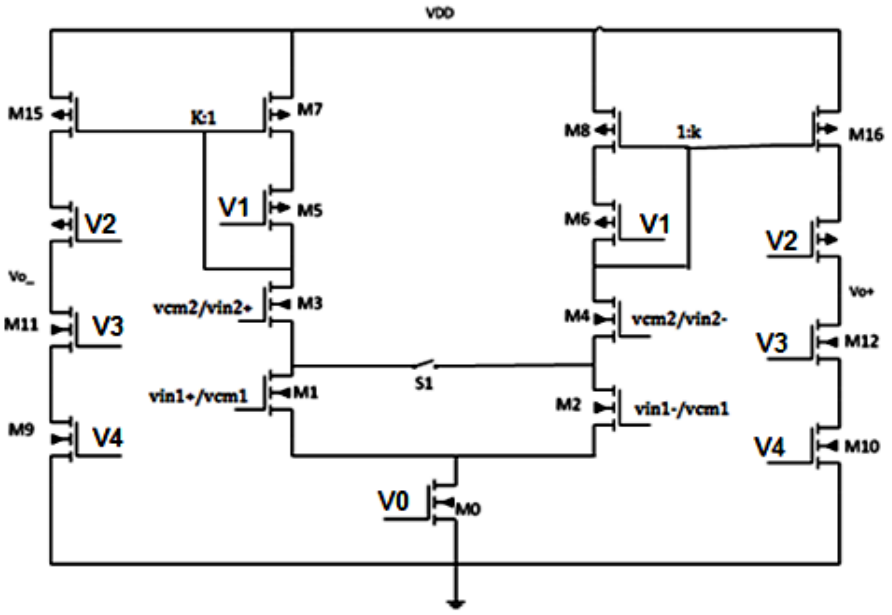


Figure 3. 1st stage of the proposed opamp

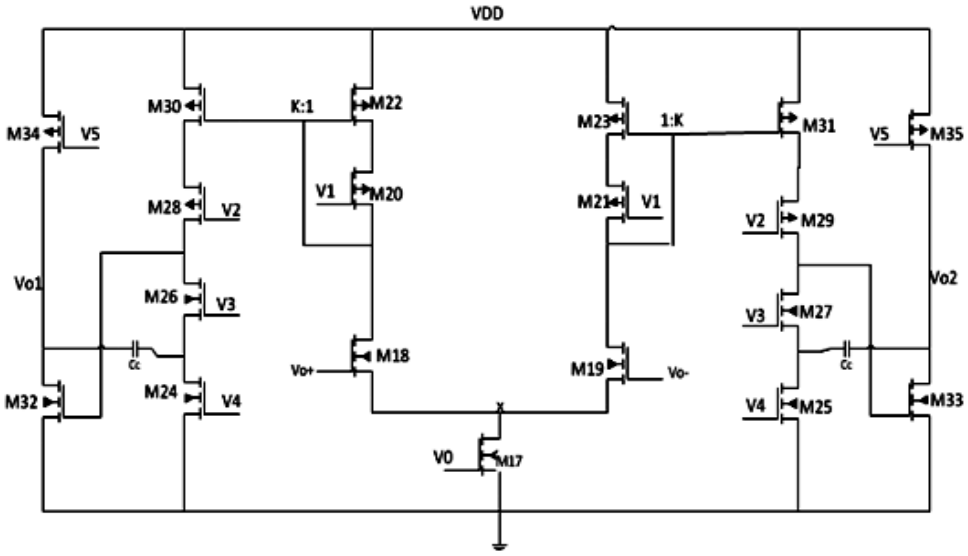


Figure 4. 2nd and 3rd stage of the proposed opamp

The charge injection and clock feedthrough of S1 in differential mode is negligible and, hence, is ignored. This can be deduced from the fact that, when this can be S1 is opened, the top plate of the sampling capacitors in the following stage are floating and any differential disturbances of the sampled output are rejected. Thus non ideal switching effects from S1 are rejected [5]. Fig.5 shows the MDAC. Where the input switches are bootstrap and other switches in MDAC are transmission switch. To achieve 200MS/s ADC with 10b accuracy, DC gain and unity gain bandwidth must be [9][12]:

$$A_{open\ loop} > 2^N \rightarrow A_{open\ loop} > 60db$$

$$GBW > \frac{N \ln(2)\, f_s}{\pi \beta} \rightarrow GBW > 882.5\ MHz$$

Where $\beta$ is a feedback factor and for 1.5- bit per stage structure is ½. The switched-capacitor common-mode feedback used for the first and the second stages of the opamp are, respectively, shown in fig.6 and fig.7. During in phase $\phi_1$ and $\phi_2$, the output of the stages 1 and 2 are clamped to $V_{cm1}$ by switches M36-37 and M38-39 and output of stage 3 is clamped to $V_{cm2}$ by switches M40-M41.

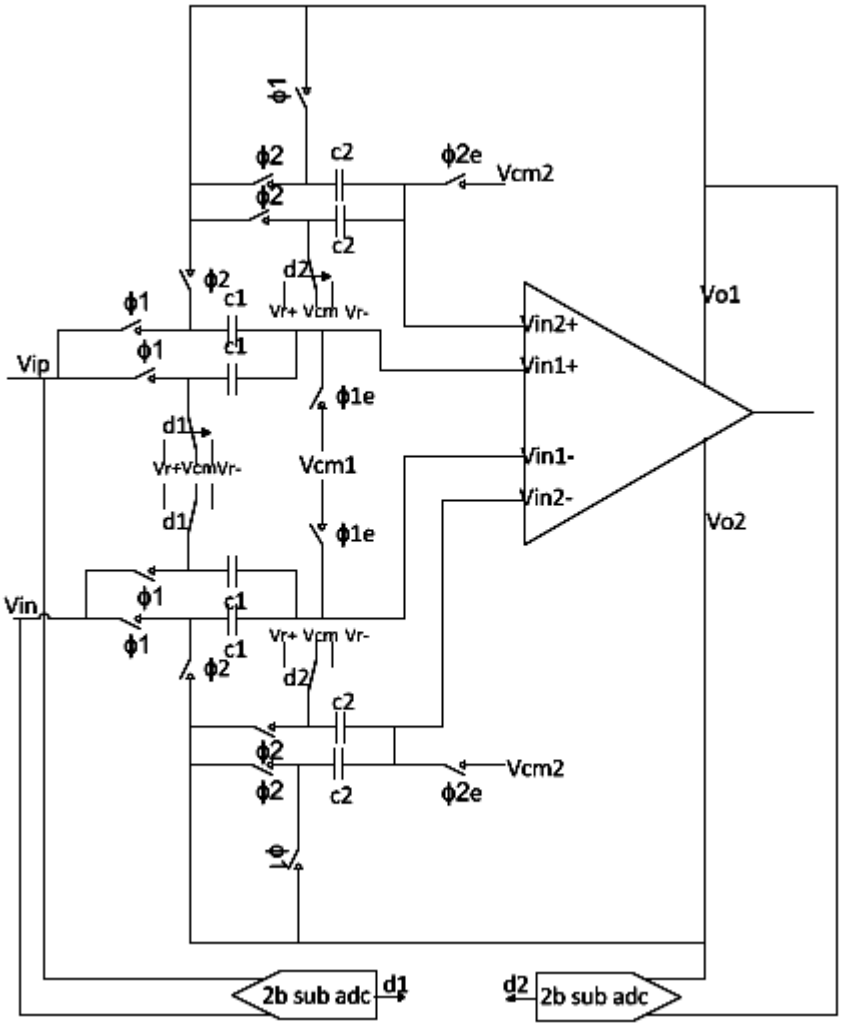


Figure 5. Schematic of opamp-sharing MDAC stage using the proposed opamp

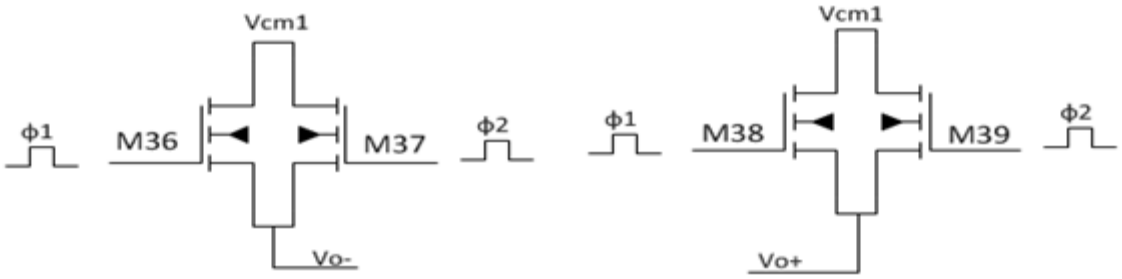


Figure 6. CMFB 1st and 2nd stage of opamp

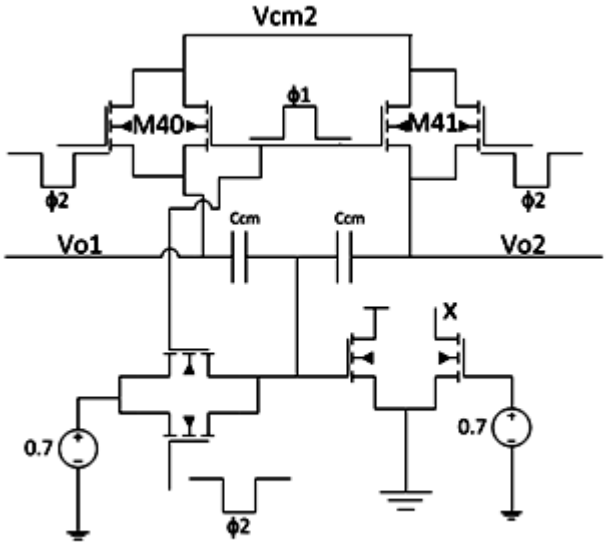


Figure 7. CMFB 1th and 2nd stage of opamp

The results of the simulation of the opamp is shown in fig.8. The gain and phase margin are 68.5dB and 74◦, respectively, and GBW is 1.3GHz.

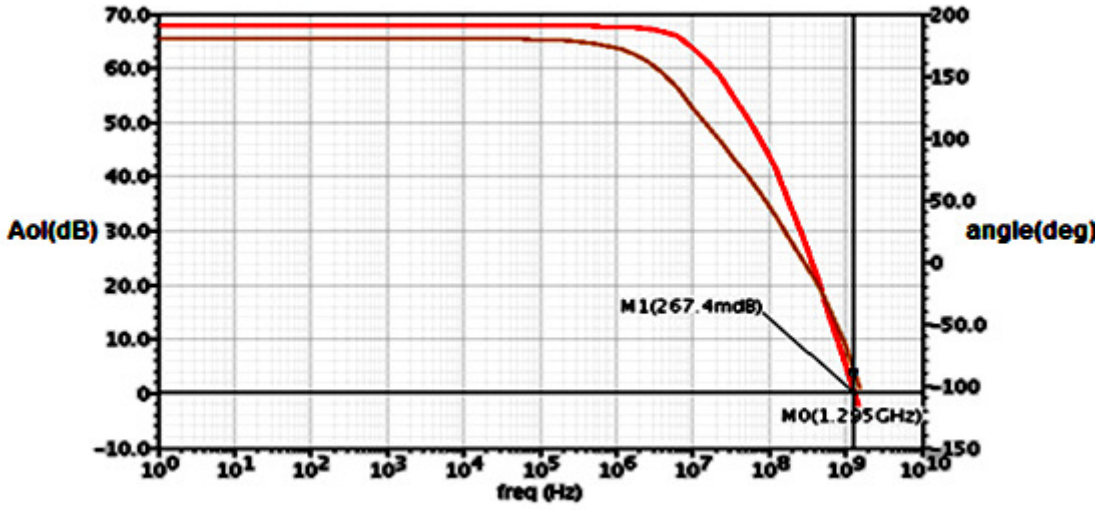


Figure 8. Simulated open-loop frequency response of proposed opamp with input pairs and capacitive load

### 3.2. Comparator

The comparator schematic used in the sub-ADC is shown in fig.9. The latch is turned on and its output is valid only during the $\phi_1$ phase of the clock [2]. When $\phi_1$ is low and the latch is reset, it is clamped to Vdd using pmos transistors. No offset cancellation scheme for the comparator is used since the overall offset variation resulted from over 200 runs of monte carlo simulation is only 13.85mV. That means that 3δ offset is 41.55mV as shown in fig.10 which is smaller than the maximum allowable value which is Vref/4 (125mV).

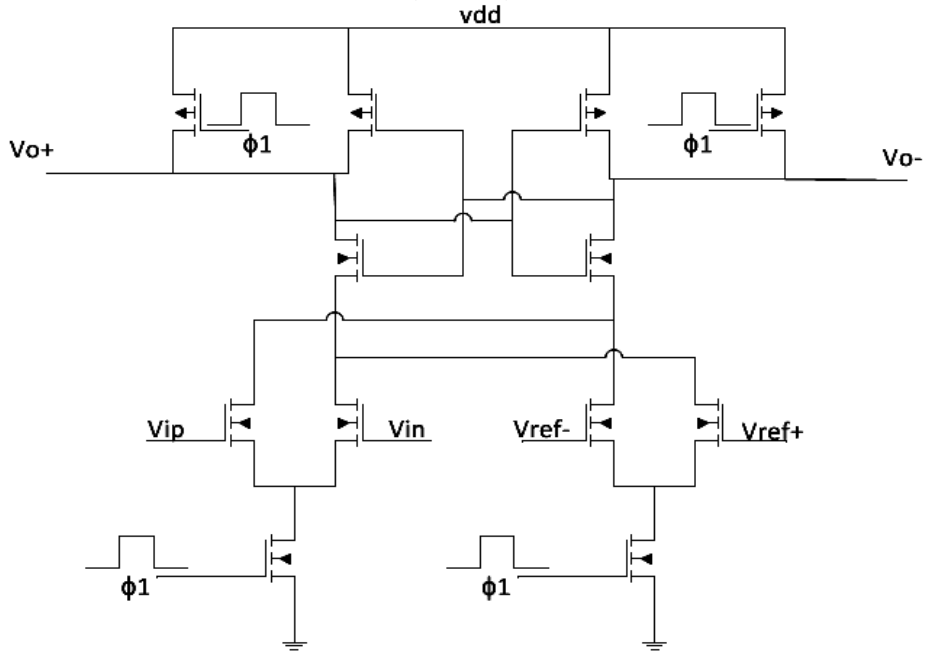


Figure 9. Schematic of comparator

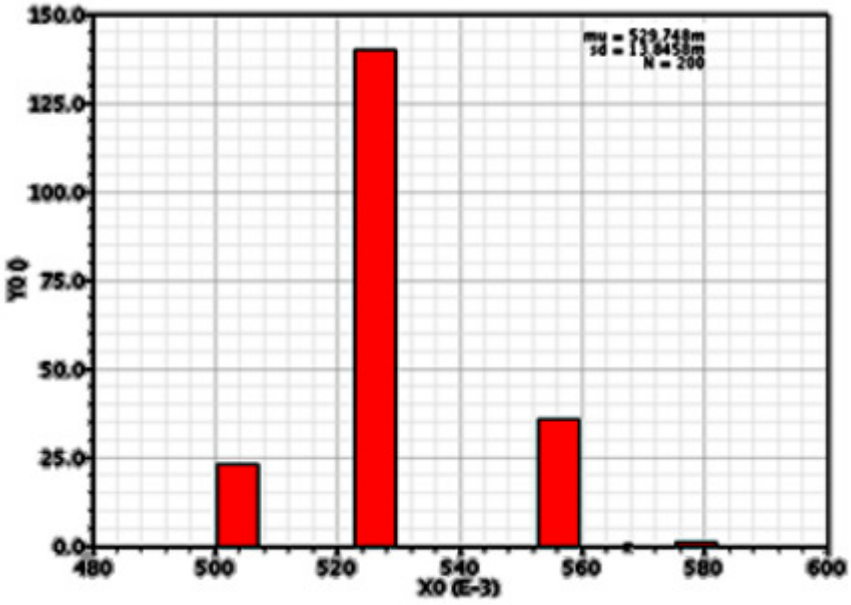


Figure 10. Monte carlo simulation of comparator

Fig.11. Summarizes the performance of comparator, where the red line represents the characteristics of the differential comparator with the threshold value of $+V_{ref}/4$.

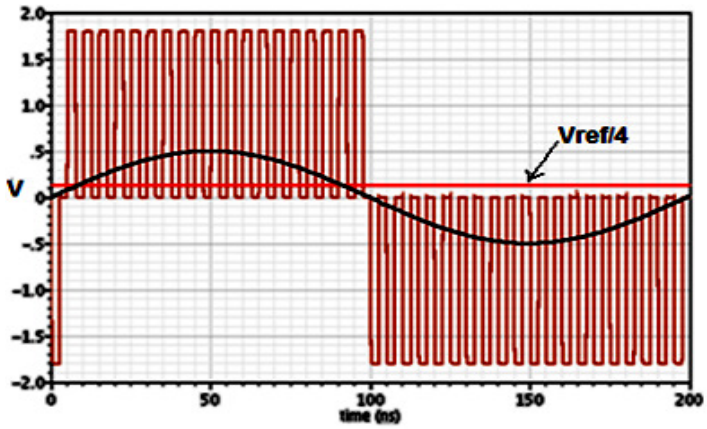


Figure 11. Performance of the comparator

## 4. CAPACITOR SCALING

For that portion of the power dissipation that is determined by capacitor, it is useful to implement a simplified analysis of noise in pipelines to find the optimum power distribution and capacitor sizing to minimize overall power. Proper capacitor scaling reduces the load capacitance on each of the op-amps, especially in the later stages. As a result, reducing the sizes of the sampling capacitors allow lower power dissipation in the later stages relative to the early stages. However, capacitor scaling in the later stages increases the noise contribution of these stages [10].

Nonetheless, since input referred noise contribution of these stages is divided by the total gain of the opamps of the previous stages, their effect is diminished. The noise contribution for each stage is:

$$V_{in,i}^2 = \frac{KT(C_{s,i}+C_{f,i}+C_{op,i})}{(C_{s,i}+C_{f,i})^2} + \left(\frac{2}{3}\right) KT \frac{1}{\beta} \frac{1}{C_{l,i}} \left(\frac{C_{s,i}}{C_{s,i}+C_{f,i}}\right) \quad (1)$$

where, K is Boltzmann constant ($1.38 \times 10^{-3}$ J/K), T is the absolute temperature, $C_{s,i}$ and $C_{f,i}$ respectively are the sampling and feedback capacitance of each stage and $C_{op}$ is the opamp parasitic capacitance. Here, $C_{s,i} = C_{f,i} = C_i$ and the value of $C_{l,i}$ is [11] :

$$C_{l,i} = C_f + \beta(C_s + C_{op}) \quad (2)$$

Since the cap is negligible, it can be ignored, resulting in.

$$V_{in,i}^2 = \frac{KT}{C_i} + \frac{1}{2} \times \frac{\frac{2}{3}KT}{C_i+\beta C_i} \frac{1}{\beta} = \frac{KT}{C_i\left(1+\frac{\frac{2}{3}}{1+\frac{1}{2}}\right)} = \frac{13KT}{9C_i} \quad (3)$$

Total input referred noise is:

$$V_{in,tot}^2 = V_{in,1}^2 + \frac{V_{in,2}^2}{G^2} + \cdots + \frac{V_{in,i}^2}{G^{2i-2}} \quad (4)$$

$$= \frac{13KT}{9}\left(\frac{1}{C_1} + \frac{1}{C_2 G^2} + \cdots + \frac{1}{C_i G^{2i-2}}\right) \quad (5)$$

where $G=\frac{1}{\beta}$. Defining scale factor $s = \frac{C_i}{C_{i+1}}$ ,one can write the above equation as:

$$V_{in,tot}^2 = \frac{13KT}{9C_1}\left(1 + \frac{s}{G^2} + \cdots + \frac{s^{i-1}}{G^{2i-2}}\right) \cong \frac{\frac{13KT}{9C_1}}{1-\frac{s}{G^2}} \quad (6)$$

the value of capacitance $C_1$ can be derived as follows:

$$V_{in,tot}^2 < V_{n,max}^2 = \frac{V_{Fs}^2}{12\times(2^N)^2} \quad (7)$$

$$\frac{\frac{13KT}{9C_1}}{1-\frac{s}{G^2}} < \frac{V_{Fs}^2}{12\times(2^N)^2} \rightarrow C_1 > 12 \times 2^{2N} \times \frac{\frac{13}{9}KT}{\left(1-\frac{s}{G^2}\right)V_{Fs}^2} \rightarrow C_1 \propto \frac{K'}{1-\frac{s}{G^2}} \quad (8)$$

$$GBW = \frac{N \ln(2) f_s}{\pi \beta} = \frac{G_{m,i}}{C_{l,i}} \rightarrow G_{m,i} = \frac{N \ln(2) f_s C_{l,i}}{\pi \beta} \quad (9)$$

$$\rightarrow G_{m,i} \propto C_{l,i} \quad (10)$$

$$P_{tot} \propto \sum G_{m,i} \propto \sum C_{l,i} \propto \sum C_{l,i} = \sum(C_{f,i} + \beta C_{s,i}) = (1+\beta)\sum C_i = (1+\beta)(C_1 + C_2 + \cdots + C_i) = (1+\beta)C_1\left(1 + \frac{1}{s} + \cdots + \frac{1}{s^i}\right) \rightarrow P_{tot} \propto \frac{C_1}{1-\frac{1}{s}} = \frac{K''}{\left(1-\frac{s}{G^2}\right)\left(1-\frac{1}{s}\right)} \quad (11)$$

$$\frac{\partial P_{tot}}{\partial s} = 0 \rightarrow s = 2 \quad (12)$$

So, to optimization of power, scaling factor, s, must be 2.

## 5. RESULTS

The 10-bit 200MS/s pipeline ADC is designed in a 0.18um CMOS process with MIM capacitors and a nominal supply of 1.8V. Fig.12 shows the FFT of the ADC output when sampling a 5.023MHz full-scale sinusoidal input at 200MS/s, and achieves an SFDR of 68.6887dB, an SNR of 60.1985dB, and SNDR of 59.4463dB. The performance of the ADC and comparison with other works is summarized in table I. The total power dissipation is 35.04mW. The worst case DNL and INL are -0.5/+0.14 LSB and -0.43/+0.4 LSB, as shown in fig.13, respectively.

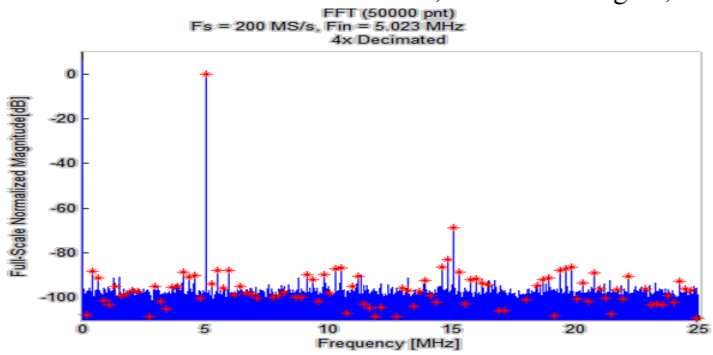


Figure 12. Measured output spectrum in 5.023MHz input at 200MS/s

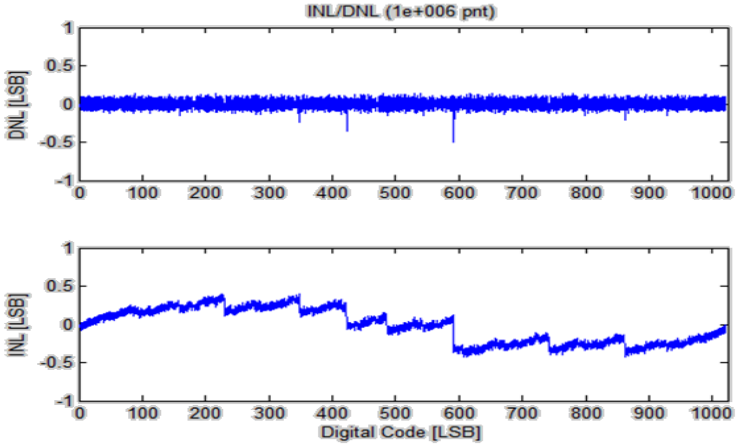


Figure 13. Measured DNL and INL of ADC

Table I. Performance summery and comparison

| Reference | [5] | [13] | [14] | This work |
|---|---|---|---|---|
| Supply voltage | 1.8V | 1.8V | 1.8V | 1.8V |
| Technology | 0.18 $\mu m\ CMOS$ | 0.18 $\mu m\ CMOS$ | 0.18 $\mu m\ CMOS$ | 0.18 $\mu m\ CMOS$ |
| Resolution | 10 bits | 10 bits | 10 bits | 10 bits |
| Convertion rate | 50 MS/s | 210 MS/s | 100 MS/s | 200 MS/s |
| Power dissipation | 9.2mW | 140mW | 67mW | 35.04mW |
| DNL | $\pm$0.4 LSB | $\pm$0.25 LSB | 0.8 LSB | -0.5/0.14 LSB |
| INL | $\pm$0.7 LSB | $\pm$0.26 LSB | 1.6 LSB | -0.43/0.4 LSB |
| SFDR | 74 dB | 85.9 dB @ $F_{in}$=20MHz | - | 68.6887 dB @ $F_{in}$=5.023MHz |
| SNDR | 58 dB | - | 54 dB | 59.4463 dB |
| SNR | 58.6 dB | 59.4 dB @ $F_{in}$=20MHz | - | 60.1985 dB @ $F_{in}$=5.023MHz |
| ENOB | - | 9.57 bits @ $F_{in}$=20MHz | - | 9.58 bits @ $F_{in}$=5.023MHz |
| FOM($\frac{\text{Power}}{2^{\text{ENOB}}\times \text{fs}}$) | 0.29 pJ/conv | - | - | 0.23 pJ/conv |

## 6. CONCLUSION

A novel mirror telescopic operational amplifier (opamp) with dual nmos differential inputs structure which alleviates memory effect and reduces the power consumption is presented. Using this architecture a 10-bit, 200MS/s, 0.18um CMOS pipeline ADC that consumes only 35.04mW, while achieving an SNDR of 59.4463dB is achieved. The design merges the front-end SHA into the first MDAC and minimize the size of the sampling capacitance in addition to sharing the opamps in order to achieve the low power consumption.

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